REMARKS

Paragraph [0001] of the specification has been amended in order to update the information respecting the referenced related application.

Claim Objections

The Examiner objected to the term "patterns which do not result in elevated quiescent levels" on the grounds that it "is unclear to what it means". The Examiner has not explained what is considered unclear. The term is intended to define test patterns which are generated, namely, test patterns that do not cause the quiescent current level of a block to rise when the test patterns are applied to the block. This limitation would exclude any generated test patterns that would cause the quiescent current level of the block to rise when the patterns applied to the block. In an attempt to clarify the objection raised by the Examiner, claims 1, 27, 42, and 68 have been amended by inserting the phrase "when applied to said block" at the locations indicated in the listing of claims.

Claim Rejections - 35 USC § 102(b)

Independent claims 1, 27, 42, 68, and a number of their dependent claims, have been rejected under 35 USC § 102(b) as being unpatentable over Deao et al. US Patent No. 6,055,649. Applicants have carefully reviewed Deao et al. and believe that Deao is cannot be considered to be an anticipation of the present invention. Reconsideration is respectfully requested in light of the following comments.

The Present Invention

The present invention is concerned with facilitating quiescent current testing of circuits which have a hierarchical architecture and hierarchical blocks which require "block specific test patterns". The method comprises the following three steps, as defined in claim 1, "for each hierarchical block which requires block specific test patterns". The first step involves:

> "configuring the block and any embedded blocks located one level down in design hierarchy in quiescent current test mode in which input peripheral memory elements are configured in internal test mode and output peripheral memory elements are configured in external test mode".

The second step involves:

> "generating quiescent current test patterns which do not result in elevated quiescent current levels when applied to said block and which include a bit for all memory elements in said block and any peripheral memory elements in any embedded blocks located one level down in design hierarchy".

The third step involves:

> "if said block contains embedded blocks, synchronizing each test pattern with a corresponding test pattern generated for embedded blocks so that test patterns loaded in scan chains in the block are consistent with test patterns loaded in scan chains in said embedded blocks."

Deao et al.

In order to anticipate the claims under rejection, the Deao reference must satisfy the well established test for anticipation outlined in MPEP 2131 as follows:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)." (emphasis added).

Deao is concerned with microprocessors having architectures with very long instruction words. As discussed in col. 4, line 65 onward, Deao seeks to provide a method in which, during the debug process of a data processing system, high speed

downloads of program memory and high speed uploads and downloads of data memory are provided so that the data streaming process according to the invention eliminates communication overhead previously associated with a serial scan test access port by providing a continuous stream of data on the scan channel of the test access port.

This is not the problem or objective with which Applicants were concerned. Conversely, Deao is not concerned with the aforementioned problem Applicants sought to overcome. Indeed, there is no mention whatever in the lengthy Deao specification of facilitating quiescent current testing of circuits, let alone of circuits having a hierarchical architecture, in which some hierarchical blocks require block specific test patterns. Thus, Applicants fail to see why one seeking a solution to the problem Applicants faced would be persuaded to refer to Deao.

The method proposed by Deao is generally described at col. 5, line 6 onward as follows:

> "A method for debugging a data processing system in which a processor has a test port for transferring data into and out of the processor includes the following steps:
> transferring first data into a first memory element within the processor via the test port;
> moving the first data from the first memory element to a different memory element accessible to said processor by executing at least one instruction within the processor in response to the step of transferring data;
> ceasing instruction execution within the processor; and
> repeating the transferring, moving and ceasing steps until a plurality of data is transferred."

This method is clearly not even remotely similar to the method set forth in the claims under rejection.

The Examiner relies on Figure 15 of the Deao drawings and the teachings in Col. 4, lines 24-40, Col. 26, lines 20-28, and Col. 1, lines 49-67 as the basis for anticipation.

Col. 4, lines 24-40 read as follows:

> "Software breakpoints (SWBP) provide another mechanism to allow the debug of microprocessor code and to evaluate performance. A SWBP is typically accomplished through opcode replacement, provided the program resides in a writable memory module which allows the opcode at the stop point to be replaced in memory with the software breakpoint

> opcode. In most machines, when a SWBP opcode reaches the first execute stage of an instruction execution pipeline, it causes the pipeline to stop advancing or trap to an interrupt service routine, and set a debug status bit indicating the pipeline has stopped or trapped. In processors classified as protected pipelines, instructions fetched into the pipeline after the SWBP are not executed. Instructions that are already in the pipeline are allowed to complete. To restart execution the pipeline can be cleared and then restarted by simply refetching the opcode at the SWBP memory address after the opcode is replaced in memory with the original opcode."

This description does not mention hierarchical blocks or embedded hierarchical blocks, configuring blocks in "quiescent current test mode" as defined in the first step of claim 1, or "generating test quiescent current test patterns .." as defined in the second step of claim 1, or "synchronizing" test patterns as required in the third step of claim 1.

Col. 26, lines 20-28 read as follows:

> "The CPU has 14 interrupts available for normal DSP operation. These are reset, the non-maskable interrupt (NMI), and interrupts 4-15. These interrupts correspond to the RESET, NMI, and INT4-INT15 signals on the CPU boundary. For some embodiments, these signals may be tied directly to pins on the device, may be connected to on-chip peripherals, or may be disabled by being permanently tied inactive on chip. Generally, RESET and NMI are directly connected to pins on the device."

As with the previous quote, this description does not mention hierarchical blocks or embedded hierarchical blocks, configuring such blocks in "quiescent current test mode" as defined in the first step of claim 1, or "generating test quiescent current test patterns .." as defined in the second step of claim 1, or "synchronizing" test patterns as required in the third step of claim 1.

Col. 1, lines 49-67 reads as follows:

> "... designed to perform. This requires verification of the design of the circuit and also various types of electrical testing after manufacture.
> However, as the complexity of the circuit increases, so does the cost and difficulty of verifying and electrically testing each of the devices in the circuit. From an electrical test standpoint, in order to totally verify that each gate in a VLSI circuit functions properly, one must ideally be

> able to exercise each of the gates not only individually (in the digital sense, determining that it is neither stuck-open nor stuck-closed), but also in conjunction with the other gates in the circuit in all possible combinations of operations. This is normally accomplished by automated testing equipment (ATE) that employs test vectors to perform the desired tests. A test vector describes the desired test input (or signals), associated clock pulse (or pulses), and expected test output (or signals) for every package pin during a period of time, often in an attempt to "test" a particular gate (or macro). For complex circuitry, this may involve a large number of test vectors ..."

Again, as with the previous quotes, this description does not mention hierarchical blocks or embedded hierarchical blocks, configuring such blocks in "quiescent current test mode" as defined in the first step of claim 1, or "generating test quiescent current test patterns .." as defined in the second step of claim 1, or "synchronizing" test patterns as required in the third step of claim 1.

Even in hindsight, which would be improper, Applicants fail to see how Deao can be considered to disclose the method set forth in the rejected claims. It is clear from the foregoing that Deao does not teach "each and every element as set forth in the claim" and does not describe the "identical invention ... in as complete detail as is contained in the claim", as required in the test for anticipation.

The same comments apply to the three other independent claims under rejection. Claim 27 is directed to a preferred embodiment of the method of the present invention. It recites the same steps as claim 1, but includes additional steps which are neither taught nor even remotely suggested by Deao. Claims 42 and 68 are directed to a "program product" for carrying out the methods of claims 1 and 27, respectively, and therefore patentably distinguish over Deao for the same reasons discussed above. The remaining rejected claims depend from one of claims 1, 27, 42 and 68 and, accordingly, they also patentably distinguish over Deao for the same reasons discussed above as well as for other reasons.

Applicants respectfully submit that all of the claims are patentable over Deao and that the application is in condition for allowance. Early favorable reconsideration and allowance of the application is respectfully requested.

Respectfully Submitted,

Eugene E. Proulx
Registration No. 35,815

e-mail: gene@logicvision.com
telephone: 613-722-2051 ext. 240